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International Bureau

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(30) Priority data:
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(71) Applicant *(for all designated States except US)*: LSI LOGIC EUROPE PLC [GB/GB]; Grenville Place, The Ring, Bracknell, Berkshire RG12 1BP (GB).

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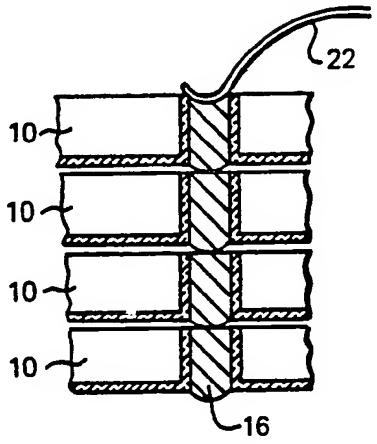
(74) Agent: THOMSON, Roger, Bruce; W.P. Thompson & Co., Eastcheap House, Central Approach, Letchworth, Hertfordshire SG6 3DS (GB).

(81) Designated States: AT (European patent), BE (European patent), CH (European patent), DE (European patent), DK (European patent), ES (European patent), FR (European patent), GB, GB (European patent), GR (European patent), IT (European patent), JP, LU (European patent), NL (European patent), SE (European patent), US.

Published
Without international search report and to be republished upon receipt of that report.

(54) Title: STACKING OF INTEGRATED CIRCUITS



(57) Abstract

An integrated circuit wafer (10) is made with a through-going plug (16) of electrically conductive material which protrudes above the wafer surface so that one can stack integrated circuits spaced from each other but interconnected electrically by the plugs (16) which extend therethrough in mutual contact.

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+ **Any designation of "SU" has effect in the Russian Federation. It is not yet known whether any such designation has effect in other States of the former Soviet Union.**

STACKING OF INTEGRATED CIRCUITS

This invention relates to the stacking of a plurality of integrated circuits on top of each other, and also to the product of that process and the intermediate product which forms part of the stack.

It is an object of the present invention to provide a method of stacking integrated circuits one on top of another in such a manner that they are electrically connected together and also in such a way that the resulting product can be processed and packaged in the normal manner using conventional assembly methods.

In accordance with the present invention there is provided an integrated circuit comprising a substrate having holes therethrough, said holes being filled with plugs of electrically conductive material which protrude above the surface of the substrate on at least one face of the substrate.

The invention also includes a stack of integrated circuits wherein the circuits are spaced from each other by the protruding plugs and are electrically interconnected by one or more such plugs of conductive material.

Also in accordance with the invention there is provided a method of fabricating a wafer for an integrated circuit which comprises the steps of making a hole through a wafer with an electrically insulating surface layer in the hole, and filling the hole with an electrically conductive material to form a plug which protrudes above the surface of the wafer on at least one face of the wafer.

Also in accordance with the present invention there is provided a method of fabricating a wafer for an integrated circuit, comprising the steps of making a

well in the wafer with an electrically insulating surface layer, filling the well with a plug of electrically conductive material, grinding the wafer to remove the wafer material below the well thereby to expose the bottom of the electrically conductive material, and providing a protruding portion of electrically conductive material at at least one end of the plug.

In order that the invention may be more fully understood, one presently preferred embodiment will now be described by way of example and with reference to the accompanying drawings, in which:

Figs. 1 to 5 show the stages in the fabrication of the intermediate product of the invention; and

Fig. 6 shows a stack of individual integrated circuit chips.

As shown in Fig. 1, the first stage in the fabrication process of a silicon wafer 10 of initial thickness T is the creation of a plurality of deep wells 12 in the silicon wafer. These can be made by a suitable etching or cutting process. The wells 12 can be purpose-designed contact areas or existing bond pad sites, and the depth of the wells will depend upon the desired final wafer thickness.

As shown in Fig. 2, the internal surface of each well 12 is coated with a suitable insulating medium to form an insulating layer 14. If the wells are cut by a laser, with oxygen present, this will form a silicon oxide layer on the surface of the well, and in this case there will be no need for a separate insulating layer 14.

As shown in Fig. 3, the wells 12 are then filled with a suitable electrically conductive material 16, up to the top surface of the wafer, to form a plug.

Next, the underside of the wafer 10 is ground away to reduce the wafer to a lesser thickness t. This exposes the conductive material 16 at the back surface of the wafer, as shown in Fig. 4.

Next, as shown in Fig. 5, the back of the wafer is covered by a suitable layer 18 of electrically insulating material and holes are made through this to the electrical contacts which are constituted by the plugs of electrically conductive material 16. After this, the back contact areas are covered by a "bump" of suitable electrically conductive material in order form a protruding pad 20. This pad 20 enables the fabricated wafer to become one component in a block or stack of wafers as shown in Fig. 6. With each pad 20 contacting the top surface of the plug of the adjacent chip one has an electrical contact which extends through the plurality of chips and forms a continuous through contact. A suitable wire bond 22 can be connected to the through contact plug. The individual chips can be stacked together after wafer sawing, or a combination of different chips can be combined together.

Although in the embodiment described above the protruding pad is at the bottom of the wafer, one could alternatively or additionally provide a protruding pad at the upper face of the wafer.

CLAIMS:

1. An integrated circuit comprising a substrate having holes therethrough, said holes being filled with plugs of electrically conductive material which protrude above the surface of the substrate on at least one face of the substrate.

2. An integrated circuit as claimed in claim 1, in which the plugs protrude above a surface of the substrate which is otherwise covered with a layer of electrically insulating material.

3. An integrated circuit as claimed in claim 1 or 2, in which the holes have an electrically insulating surface layer.

4. A stack of integrated circuits as claimed in any preceding claim, wherein the circuits are spaced from each other by the protruding plugs and are electrically interconnected by one or more such plugs of conductive material.

5. A method of fabricating a wafer for an integrated circuit which comprises the steps of making a hole through a wafer with an electrically insulating surface layer in the hole, and filling the hole with an electrically conductive material to form a plug which protrudes above the surface of the wafer on at least one face of the wafer.

6. A method of fabricating a wafer for an integrated circuit, comprising the steps of making a well in the wafer with an electrically insulating surface layer, filling the well with a plug of electrically conductive material, grinding the wafer to remove the wafer material below the well thereby to expose the bottom of the electrically conductive material, and providing a protruding portion of electrically conductive material at at least one end of

the plug.

7. A method as claimed in claim 6, which includes coating the wafer material around the exposed bottom of the plug with a layer of electrically insulating material.

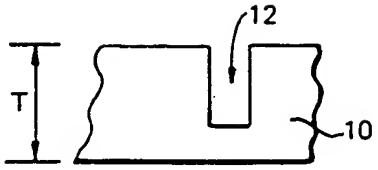

FIG. 1

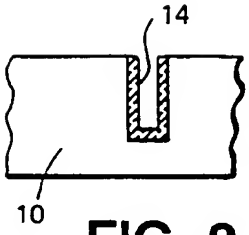

FIG. 2

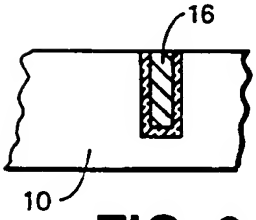

FIG. 3

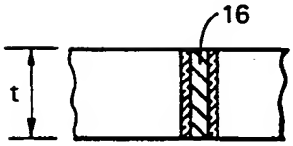

FIG. 4

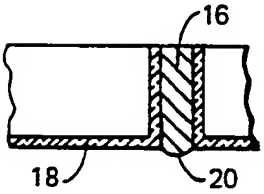

FIG. 5

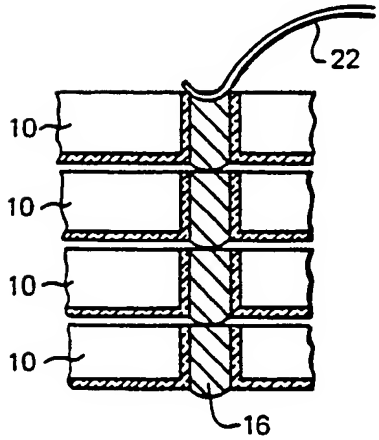

FIG. 6

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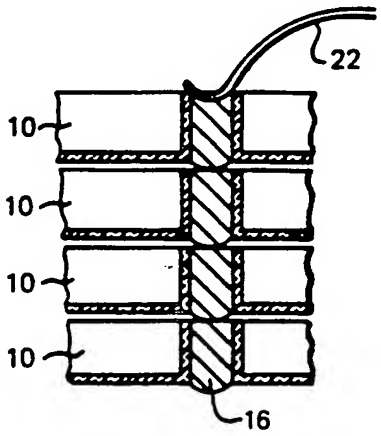
(54) Title: STACKING OF INTEGRATED CIRCUITS



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DE	Germany	LU	Luxembourg	TG	Togo
DK	Denmark	MC	Monaco	US	United States of America

INTERNATIONAL SEARCH REPORT

International Application No PCT/GB 91/01459

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)[6]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int.Cl.5 H 01 L 25/065

II. FIELDS SEARCHED

Minimum Documentation Searched[7]

Classification System	Classification Symbols
Int.Cl.5	H 01 L

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched[8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT[9]

Category °	Citation of Document,[11] with indication, where appropriate, of the relevant passages[12]	Relevant to Claim No.[13]
X	EP,A,0314437 (LASER DYNAMICS) 3 May 1989, see whole document	1-5
X	US,A,4897708 (K. CLEMENTS) 30 January 1990, see column 3, line 6 - column 4, line 22; column 5, lines 29-52; figures 1-8; claims 1,8,11	1-5
X	DE,A,3233195 (MITSUBISHI DENKI) 17 March 1983, see whole document	1,2,4

° Special categories of cited documents :[10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
12-12-1991	12. 06. 92
International Searching Authority: EUROPEAN PATENT OFFICE	Signature of Authorized Officer: Danielle van der Haas

Form PCT/ISA/210 (second sheet) (January 1985)

FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET

V. ☐ OBSERVATION WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE [1]

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claim numbers because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claim numbers because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claim numbers because they are dependent claims and are not drafted in accordance with the second and third sentences of PCT Rule 6.4(a).

VI. ☒ OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING [2]

This International Searching Authority found multiple inventions in this international application as follows:

1. Claims 1-5
2. Claims 6,7

For further information please see form PCT/ISA/206 dated by 14.02.1992

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims of the international application

2. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims of the international application for which fees were paid, specifically claims:

3. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers:

4. ☐ As all searchable claims could be searched without effort justifying an additional fee, the International Searching Authority did not invite payment of any additional fee.

Remark on Protest

☐ The additional search fees were accompanied by applicant's protest.

☒ No protest accompanied the payment of additional search fees.

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO. GB 9101459 SA 50890

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 26/05/92
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP-A- 0314437	03-05-89	JP-A- 2001152	05-01-90
US-A- 4897708	30-01-90	US-A- 4954875	04-09-90
DE-A- 3233195	17-03-83	JP-A- 58043554	14-03-83